

# PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

## TABLE OF CONTENTS

Page Description

1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCI Termination
5	MEMORY: GPU Partition A/B
6	MEMORY: FBA Partition 31..0
7	MEMORY: FBA Partition 63..32
8	MEMORY: FBB Partition 31..0
9	MEMORY: FBB Partition 63..32
10	MEMORY: GPU Partition C/D
11	MEMORY: FBC Partition 31..0
12	MEMORY: FBC Partition 63..32
13	MEMORY: FBD Partition 31..0
14	MEMORY: FBD Partition 63..32
15	GPU PWR and GND
16	GPU Decoupling
17	GPU DECOUPLING
18	IFPAB TALL-DP
19	IFPE DP
20	IFPF USBC
21	IFPC HDMI 2.0/DP
22	IFPD DP
23	NVHS INTERFACE
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO
25	MISC3: ROM, STRAPS

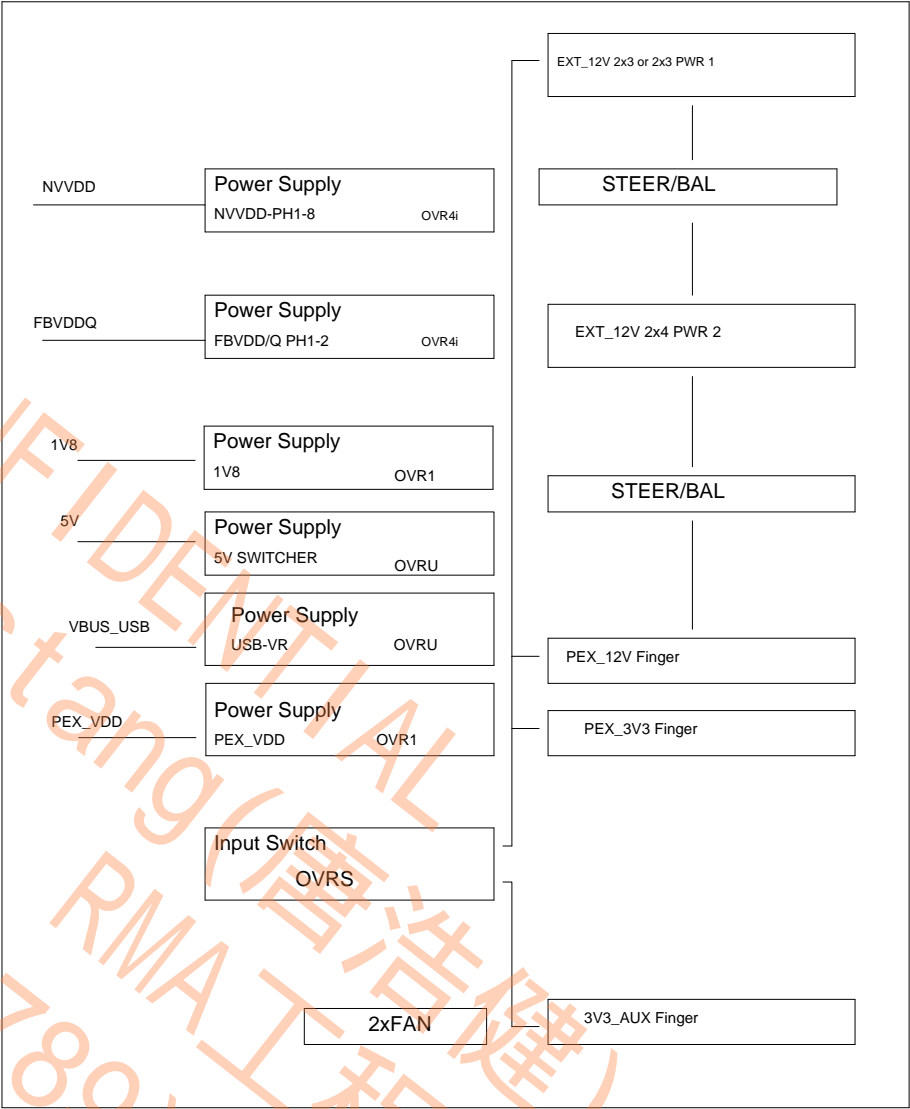
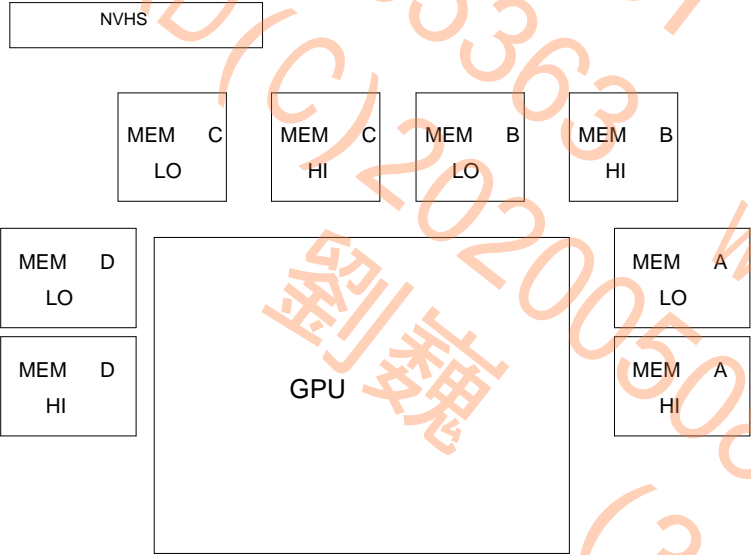
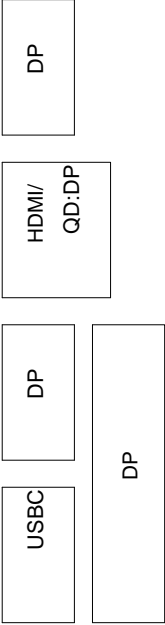
Page Description

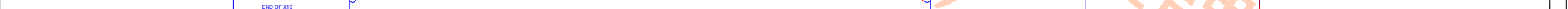
26	MISC: XTAL, PLL
27	MISC: USB PPC
28	PS: USB VR
29	PS: 5V, 5V BACKUP
30	PS: PEXVDD, 1V8
31	PS: FBVDD CONTROLLER
32	PS: FBVDD CONTROLLER OVR3
33	PS: FBVDD PHASE 1, 2
34	PS: NVVDD CONTROLLER OVR8
35	PS: NVVDD Phase 1, 2
36	PS: NVVDD Phase 3, 4
37	PS: NVVDD Phase 5, 6
38	PS: NVVDD Phase 7, 8
39	PS: INPUT SWITCH RTD3
40	PS: INPUT SWITCH RTD3 USB
41	PS: INPUT SWITCH RAIL BALANCE
42	PS: 12V CURRENT STEERING
43	PS: VR THERMAL PROTECTION
44	PS: INPUTS, FILTERING AND MONITORING
45	PS: CURRENT STEERING,HOT UNPLUG DETECT
46	PS: PRE-FILTER
47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE
48	SEQUENCE: NV, PEX, FB ENABLE
49	SEQUENCE: PCIE VOLTAGE MONITOR
50	SEQUENCE: DISCHARGE

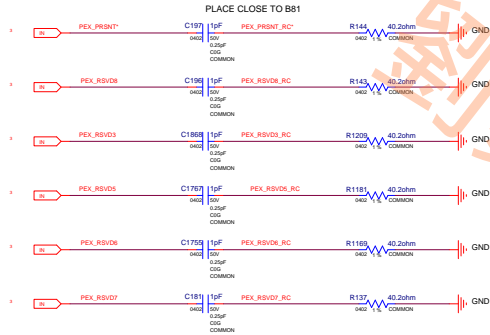
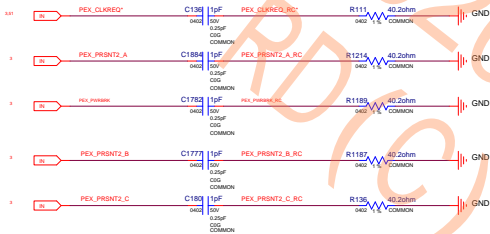
Page Description

51	SEQUENCE: MISC
52	LED & FAN HEADERS
53	LED 2
54	Mechanical: Bracket/Thermal Solution

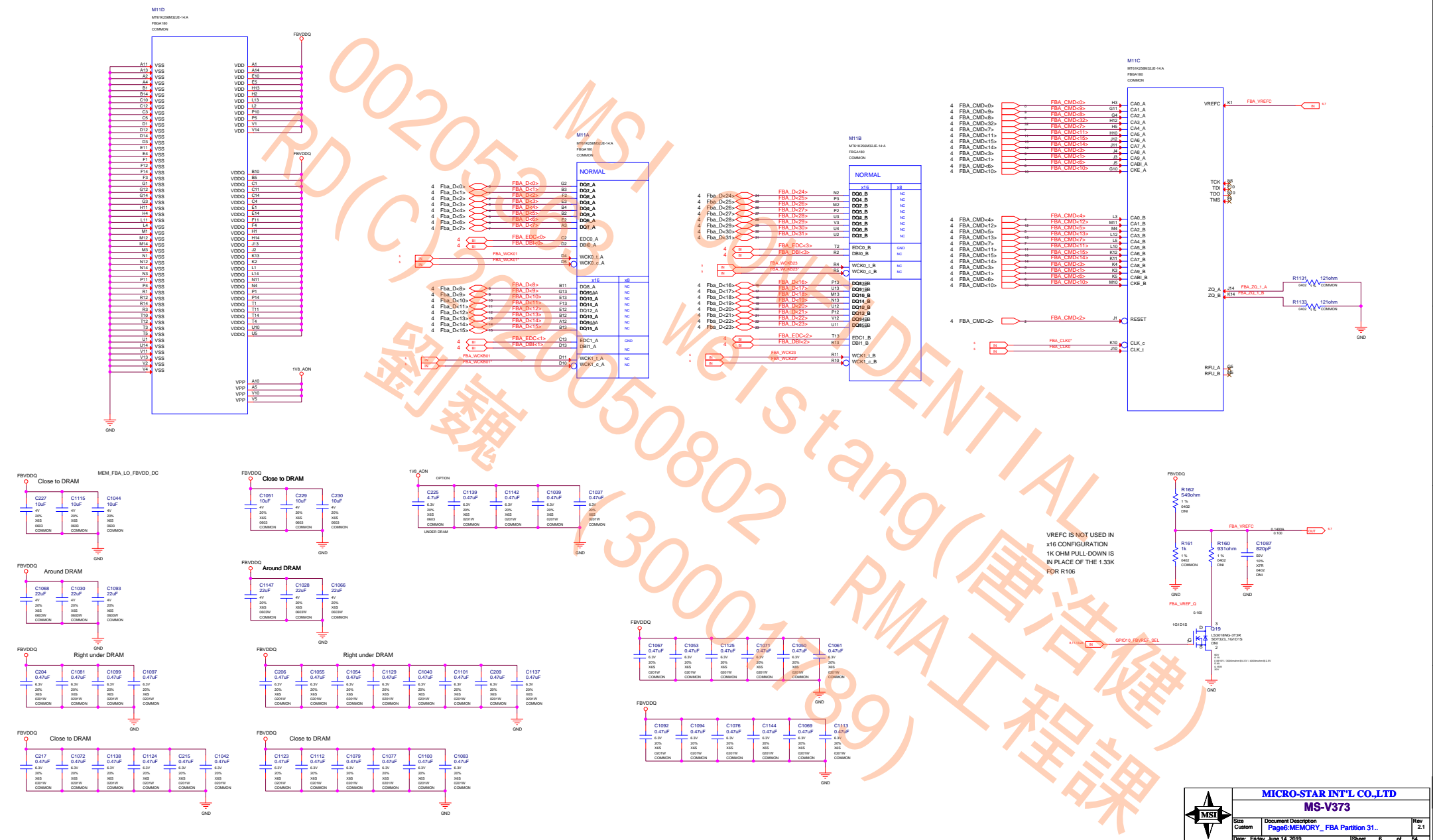
base on V372-02S change for D18 Z  
 1. P.23 remove SL1 & BRIDGE LED\_VDD & SL1\_BRG\_PRST\*  
 2. P.52 remove LED change FAN connector  
 3. P.53 remove LED  
 4. P.38/44 add FUSE  
 5. P.5~14 mem add <>  
 6. P.53 LED use V336-0D  
 7. P.32 remove  
 8. P.35~38 dual MOS  
 9. P.33 change dual MOS  
 10. P.43 remove  
 11. P.31 change to UP1666  
 12. P.21 remove colay DP  
 2019/06/17  
 1.add NV link

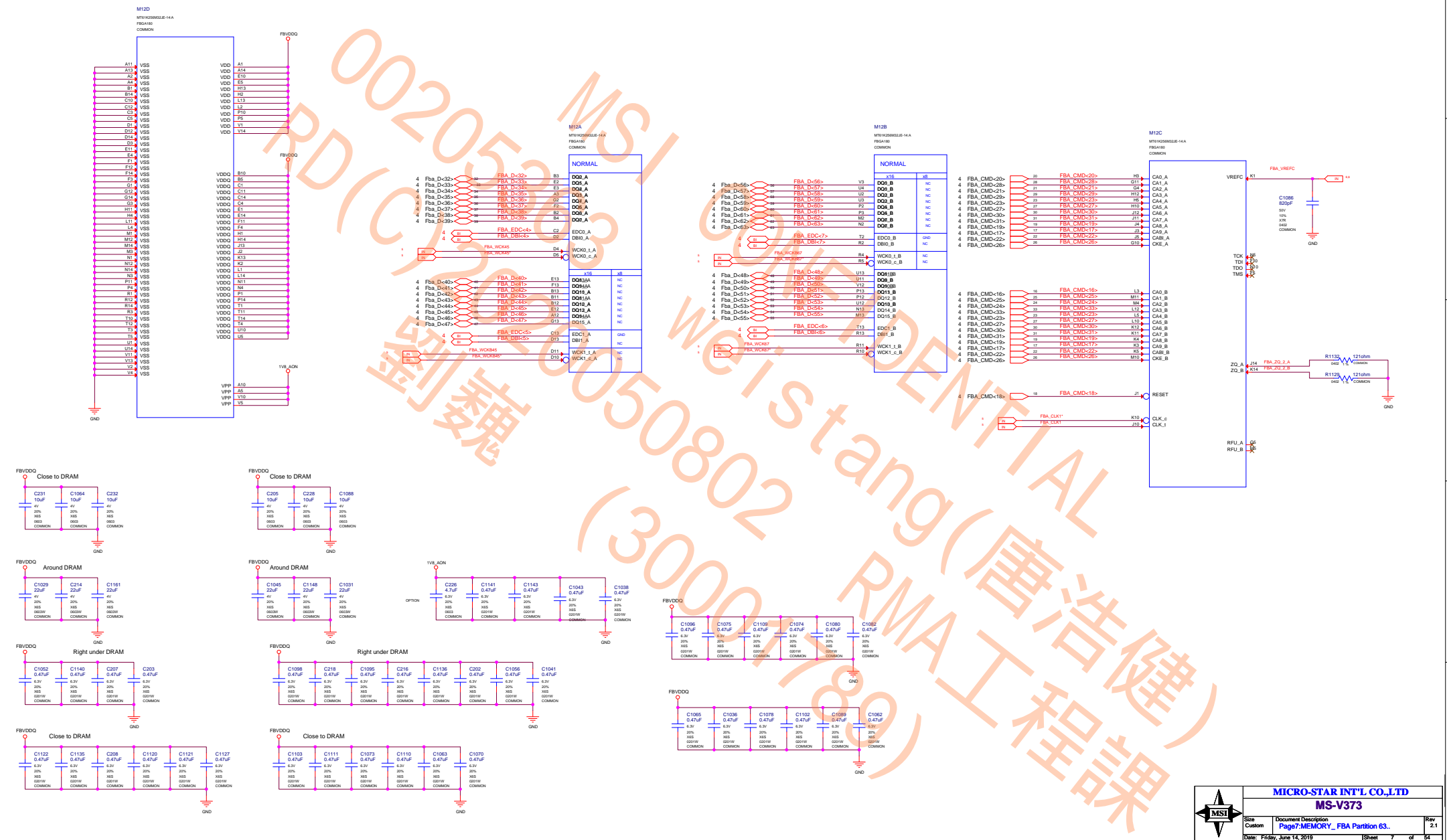




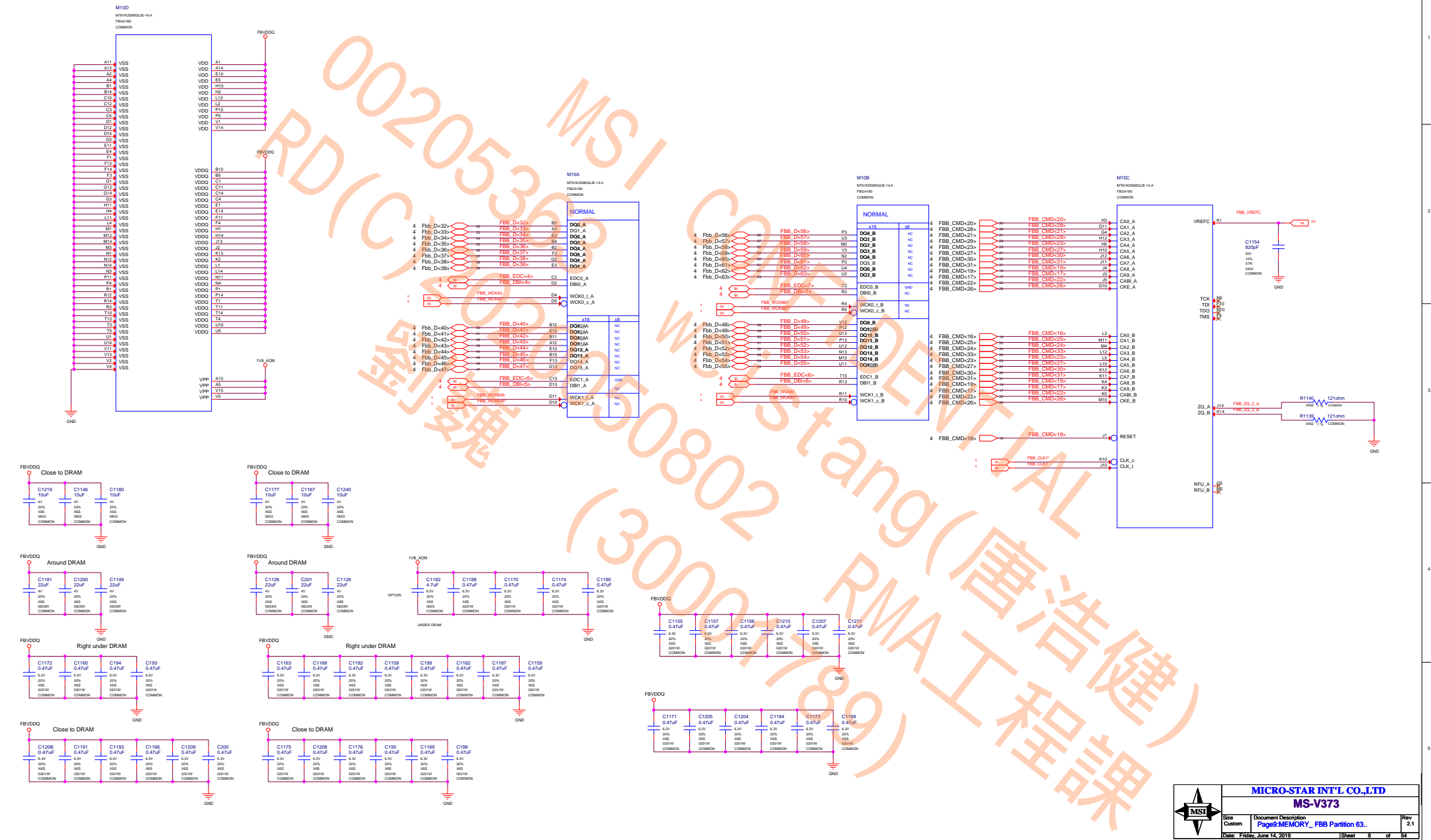


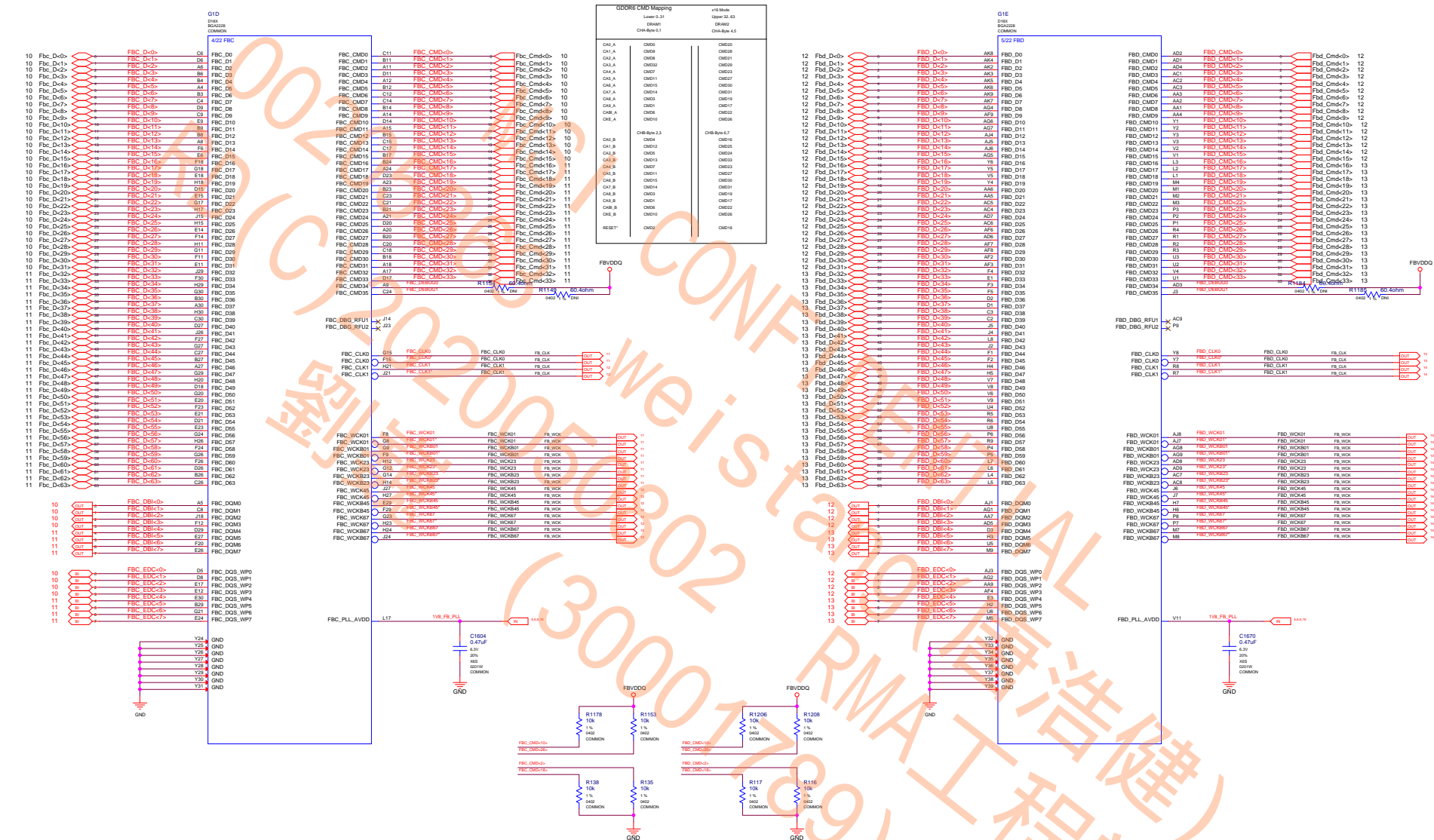


















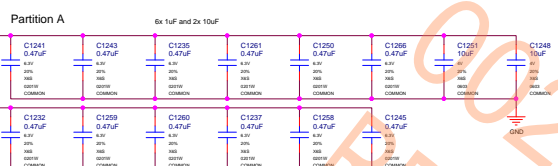




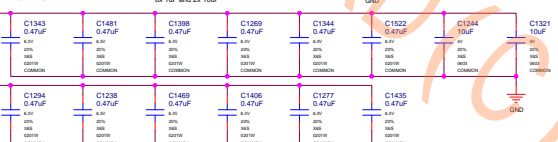
## NVVDD

## FBVDDQ

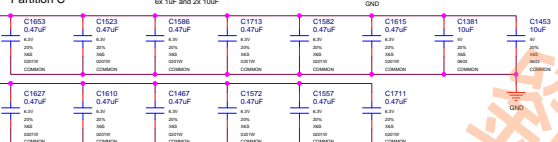
## Partition A



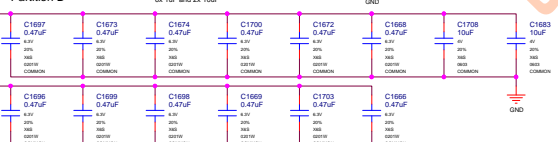
## Partition B



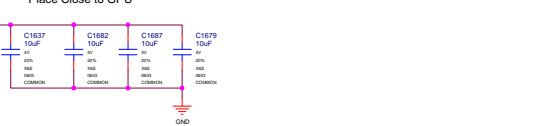
## Partition C



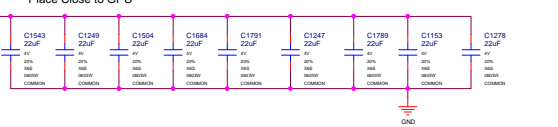
## Partition D



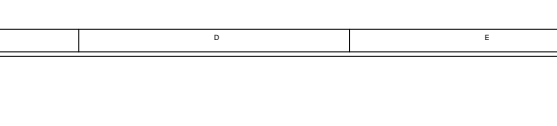
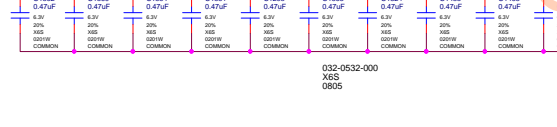
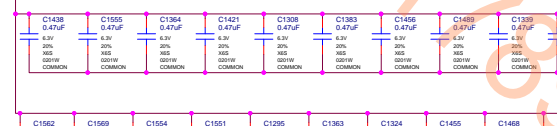
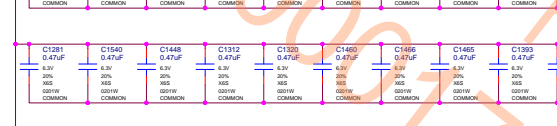
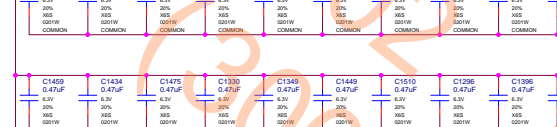
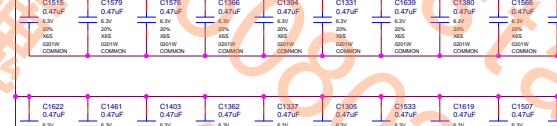
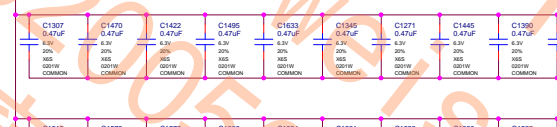
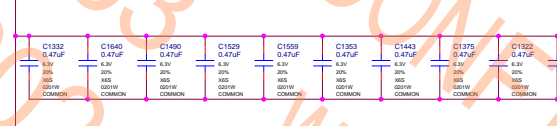
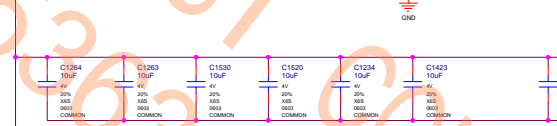
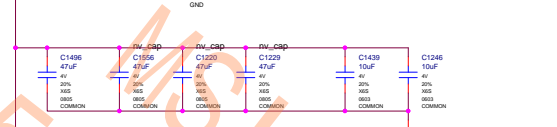
## Place Close to GPU



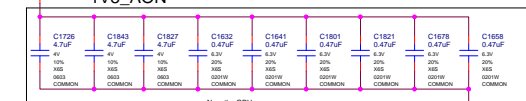
## Place Close to GPU



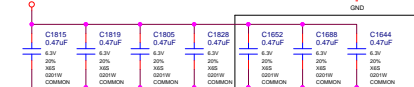
## NVVDD

032-0532-000  
XES  
0805

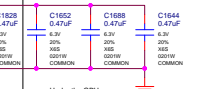
## 1V8\_AON



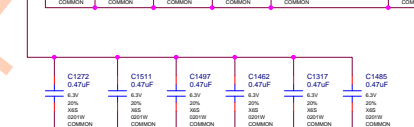
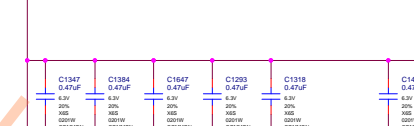
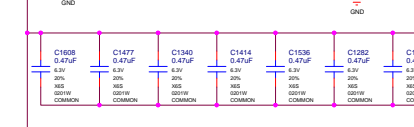
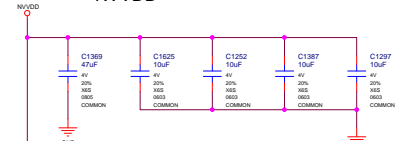
## Near the GPU



## Under the GPU



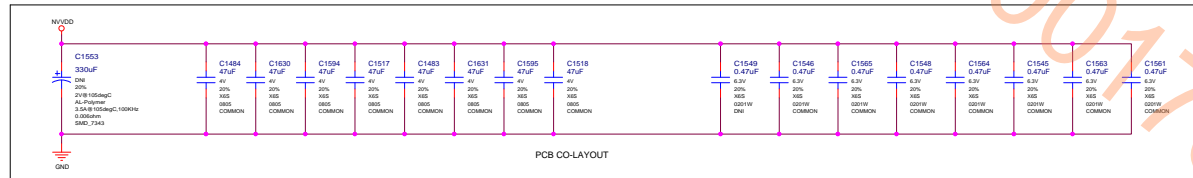
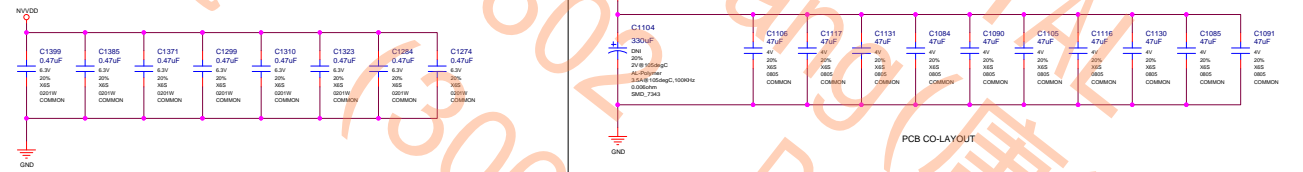
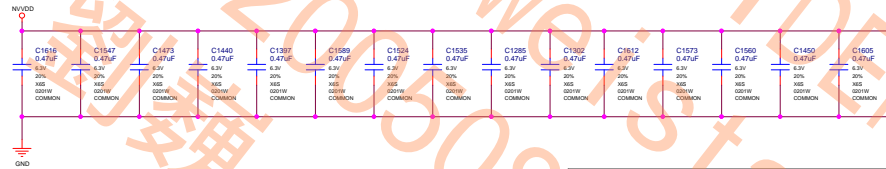
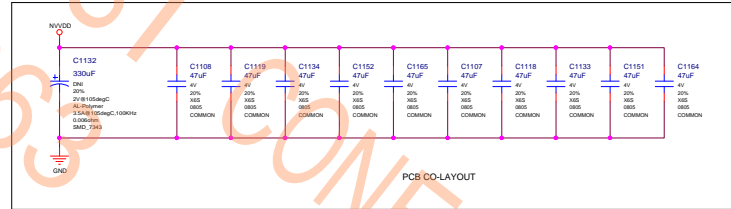
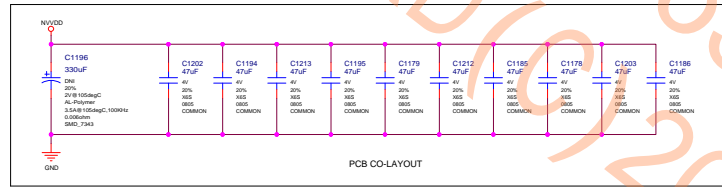
## NVVDD



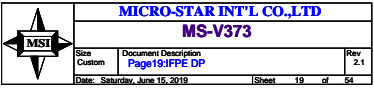
MICRO-STAR INT'L CO., LTD

MS-V373

Size: Custom Document Description: Page16:GPU Decoupling Rev: 2.1 Date: Friday, June 14, 2019 Sheet: 16 of 54

















H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

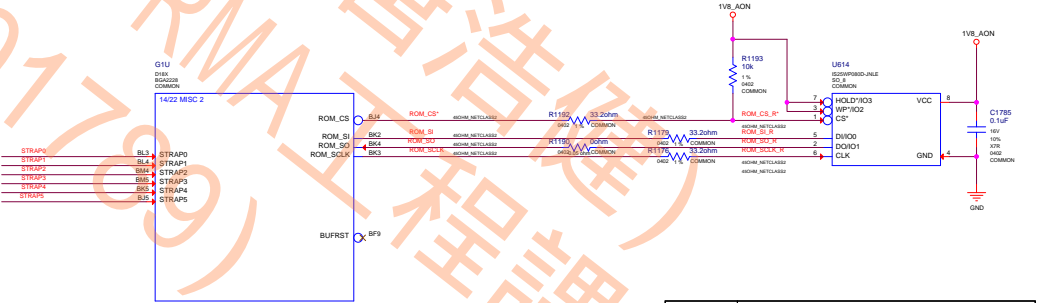
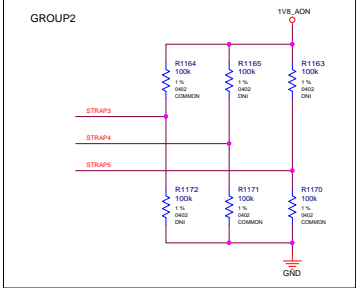
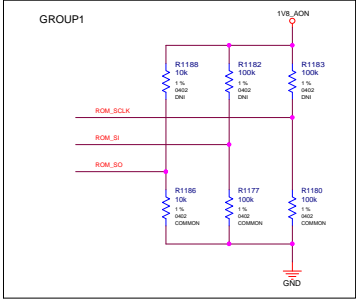
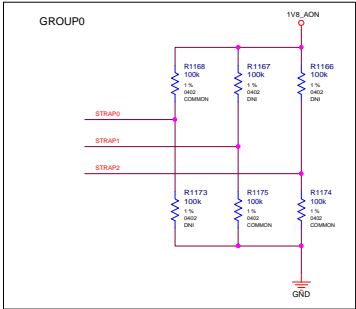
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung















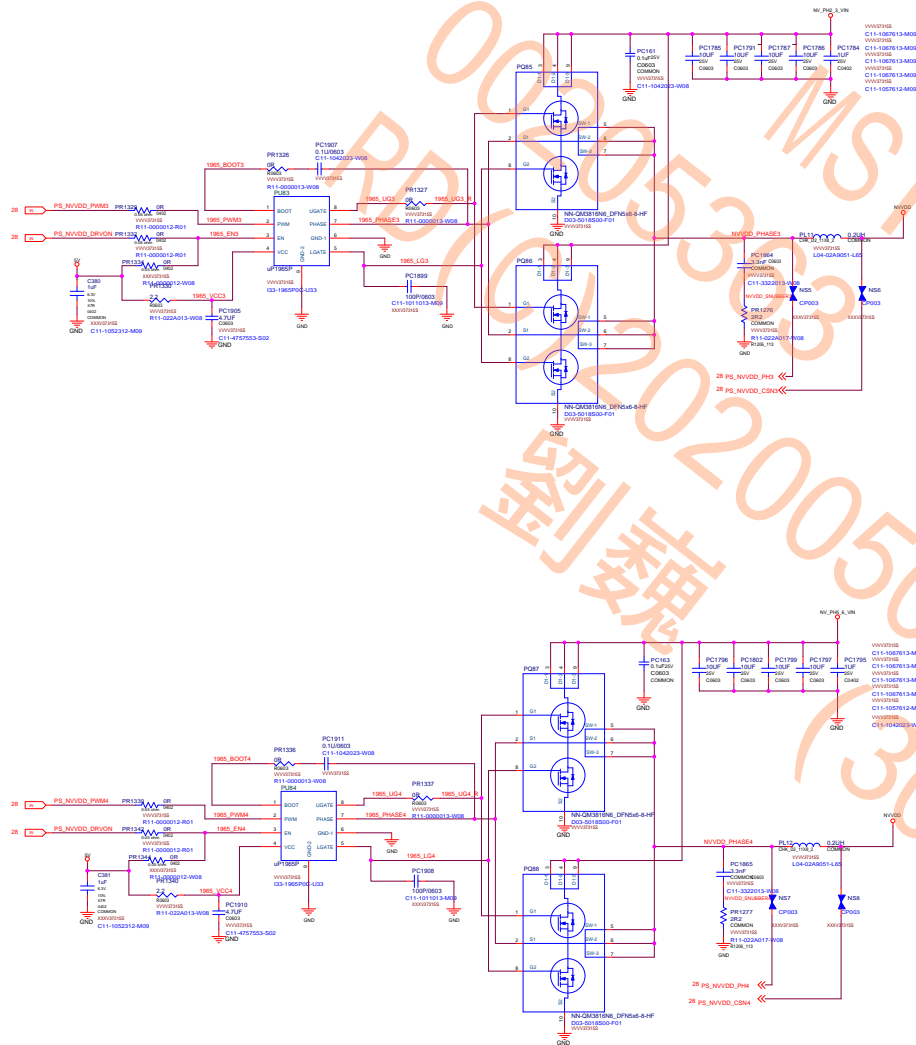
MSI CONFIDENTIAL  
00205363  
RD(C)2020050802  
劉魏  
weistang (唐浩健)  
(30001789)  
RMA工程課

MICRO-STAR INT'L CO.,LTD		
MS-V373		
Size	Document Description	Rev
Custom	Page32:PS_FBVD Controller OVR3	2.1
Date: Friday, June 14, 2019		Sheet 32 of 54











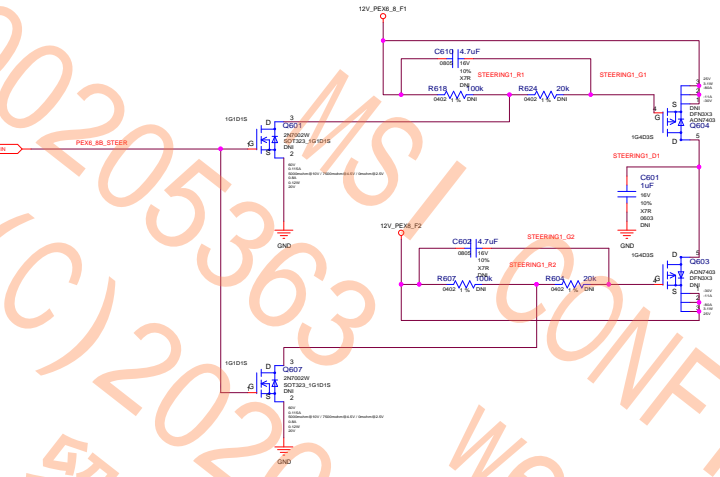




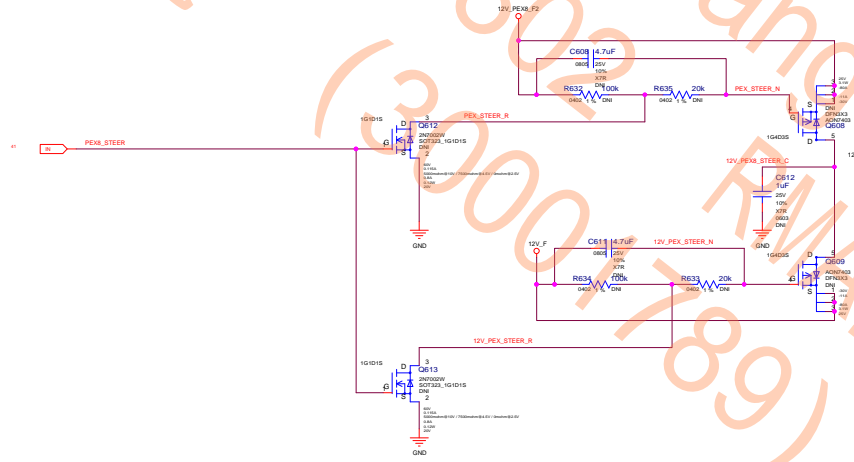




12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



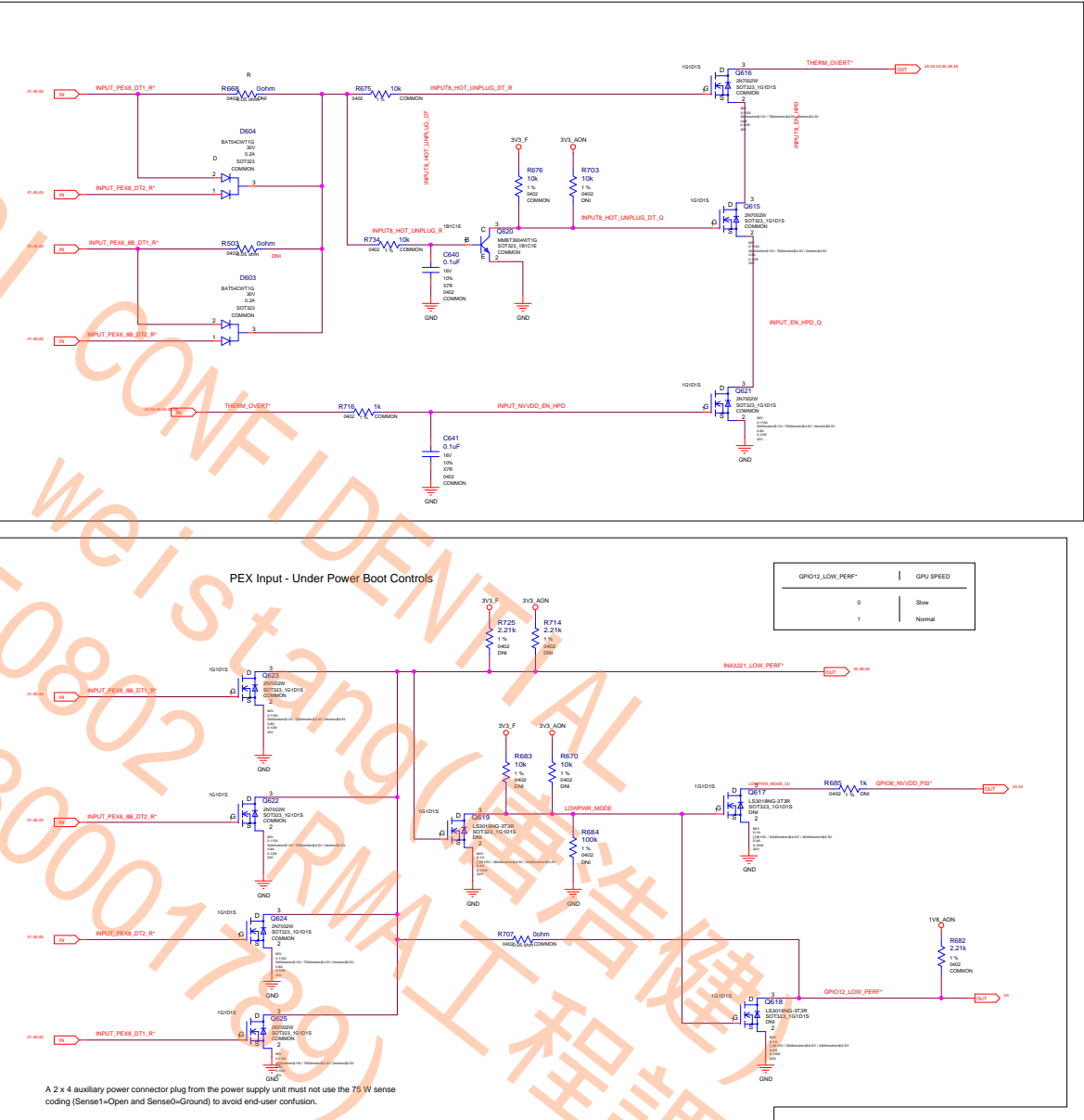
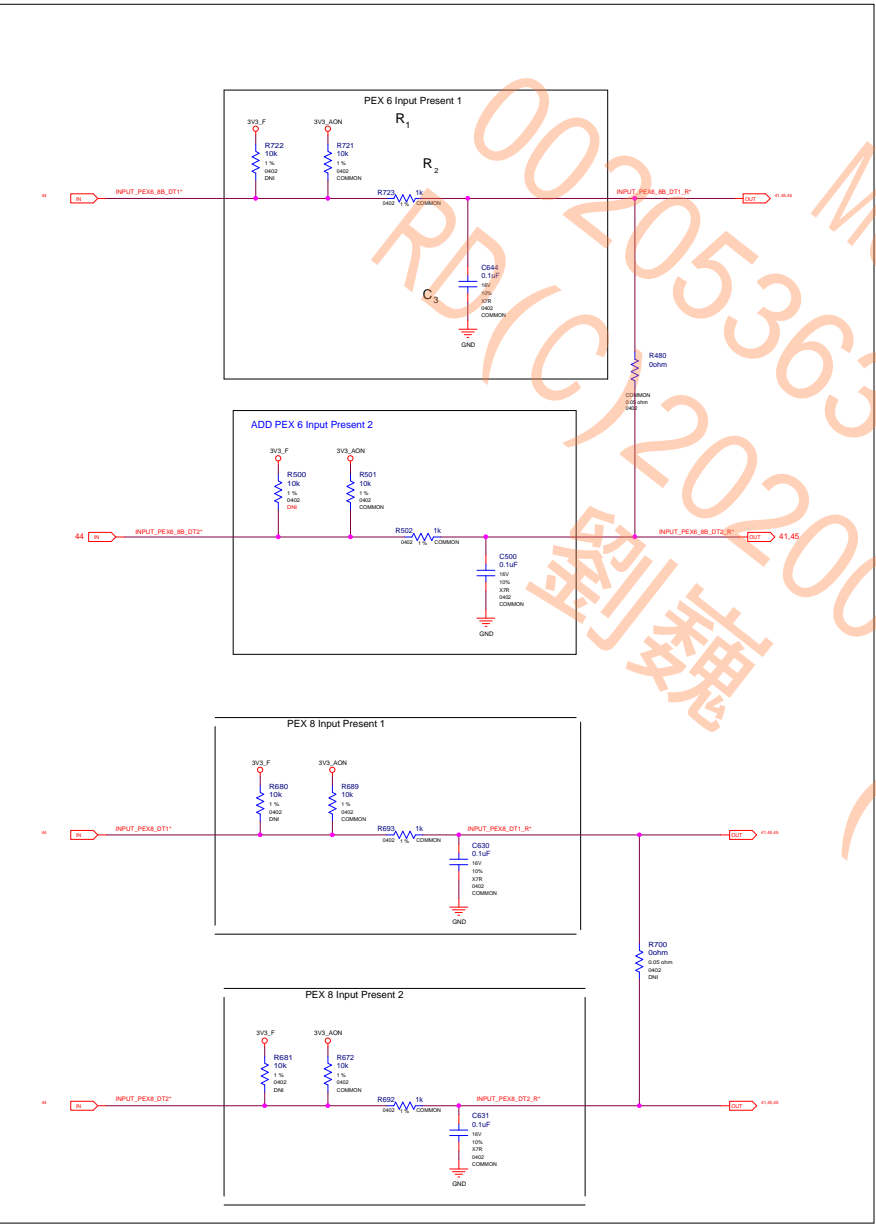
12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



MSI CONFIDENTIAL  
00205363  
RD(C)2020050802  
劉魏  
weistang(唐浩健)  
(30001789)  
RMA工程課

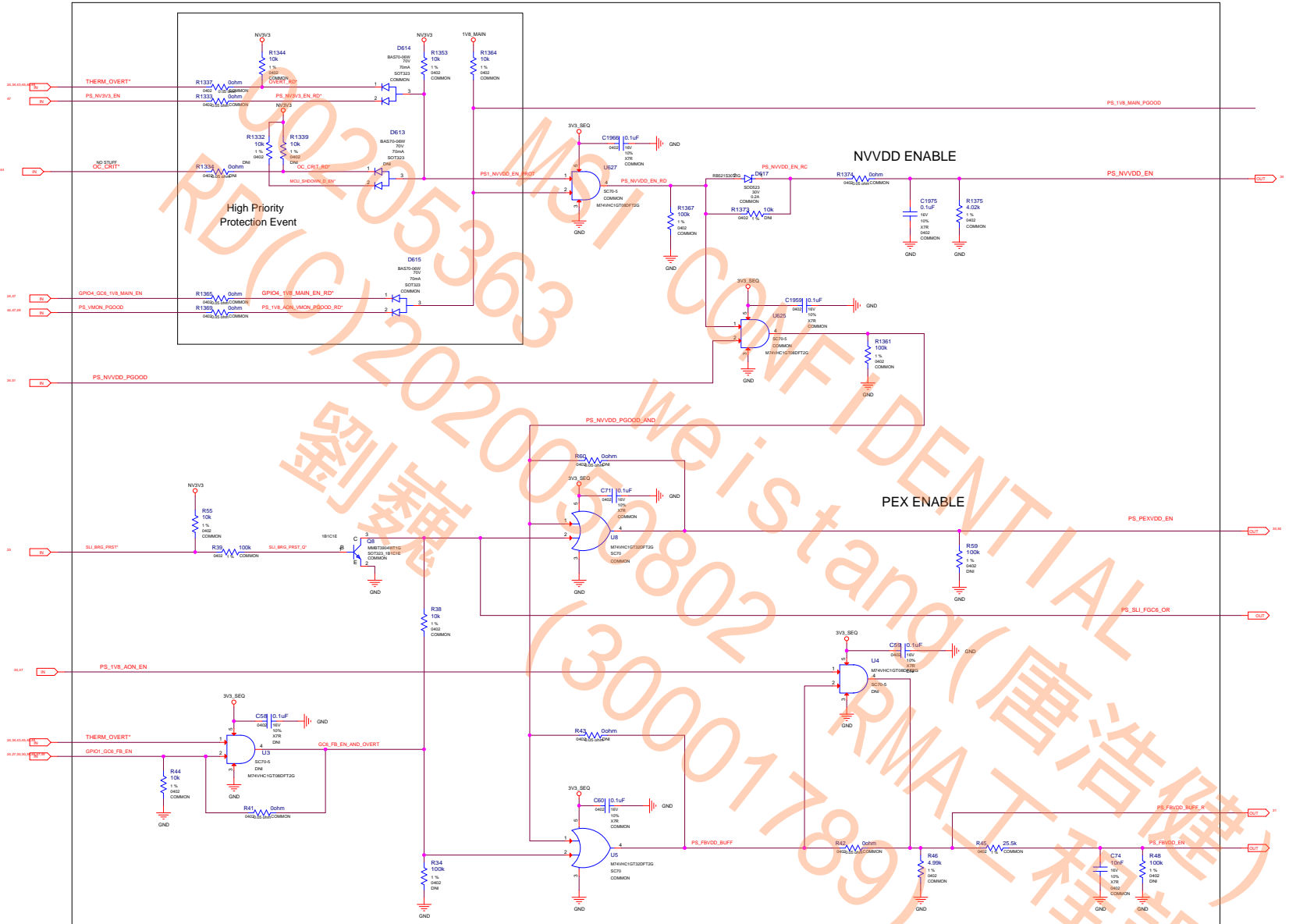
MICRO-STAR INT'L CO.,LTD		
MS-V373		
Size	Document Description	Rev
Custom	Page43.PS_VR THERMAL PROTECTION	2.1
Date: Friday, June 14, 2019		Sheet 43 of 54



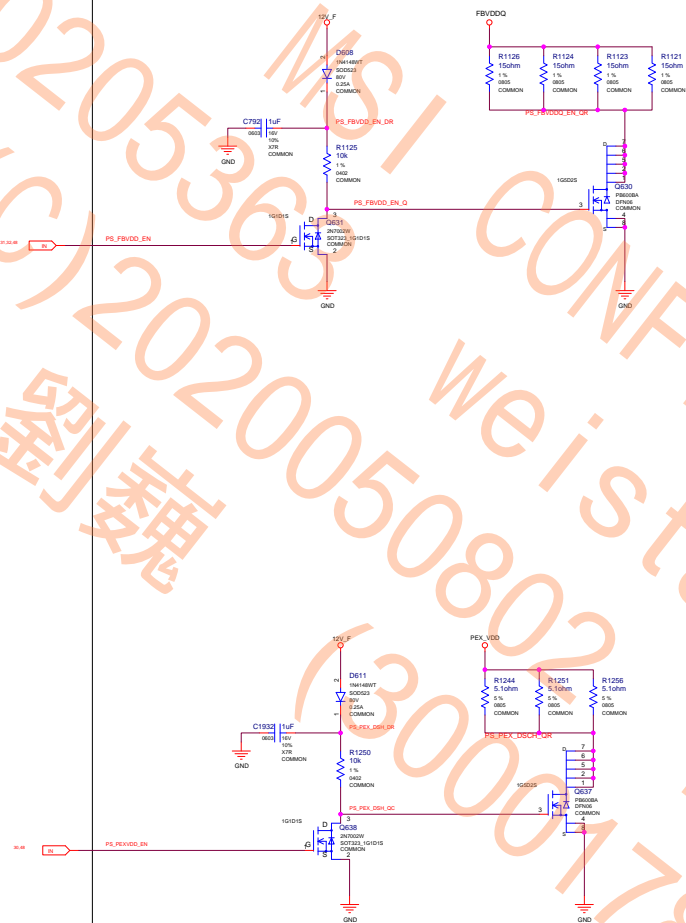


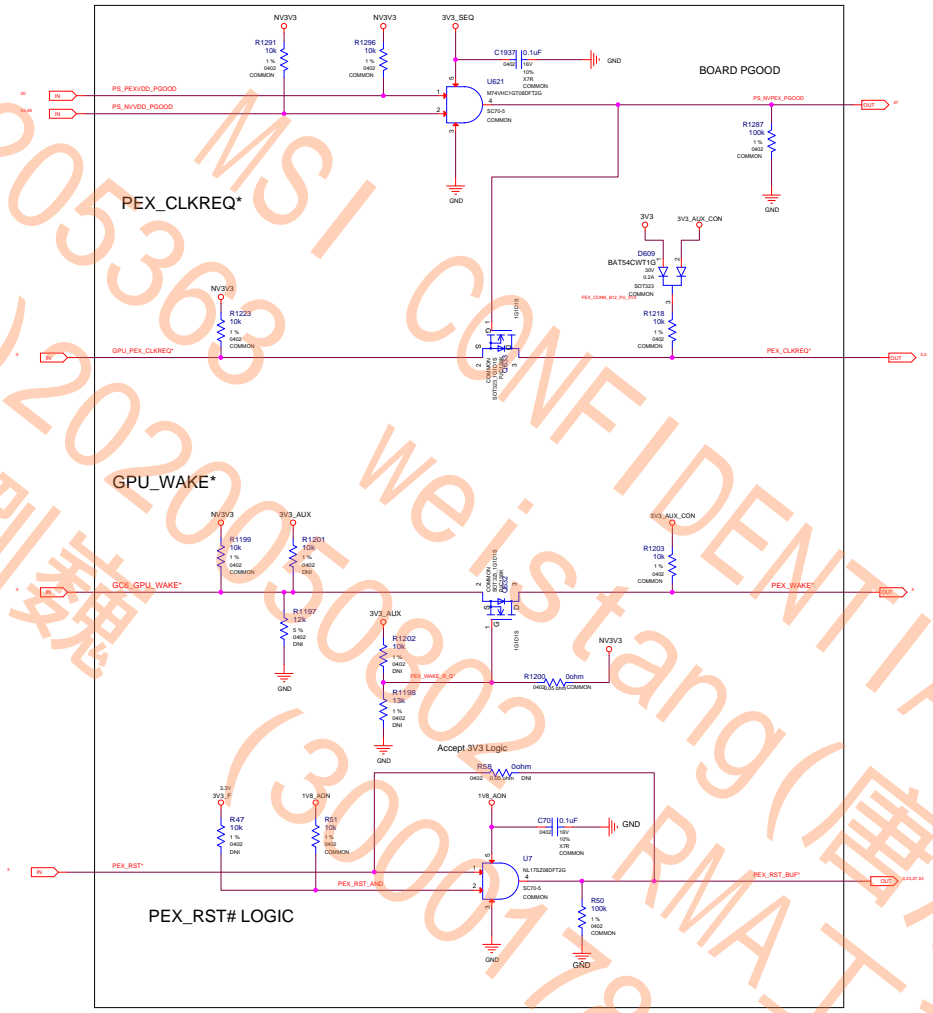


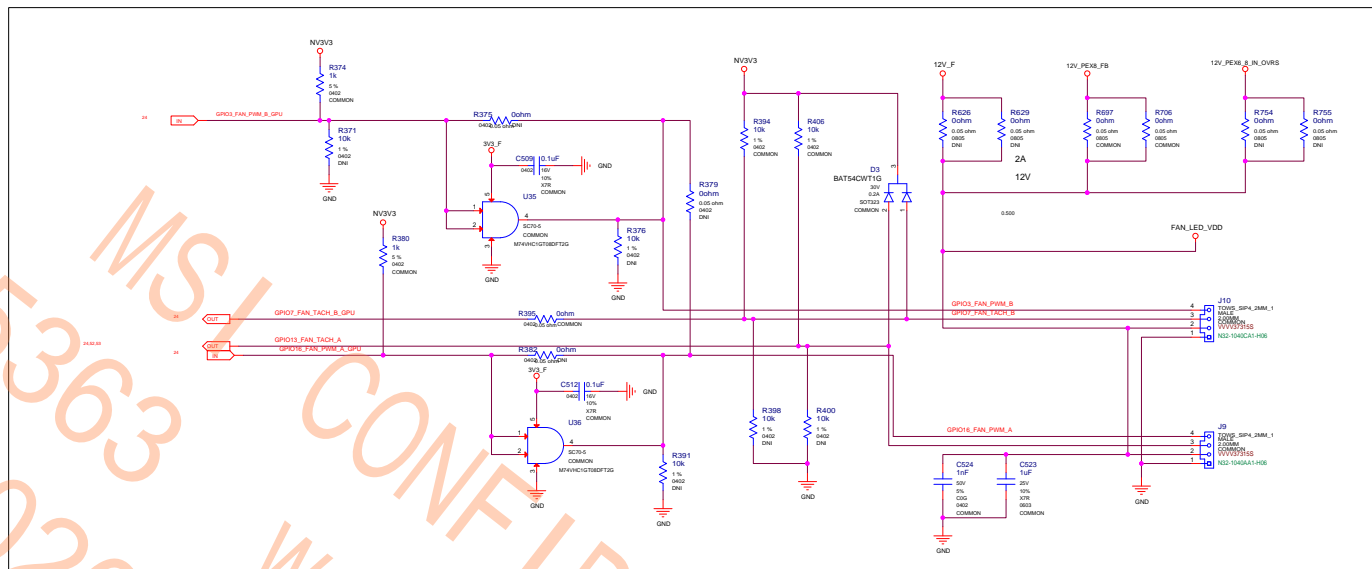










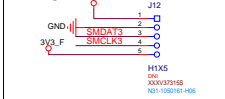


LED BOOST

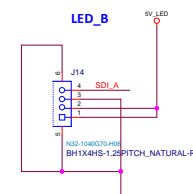
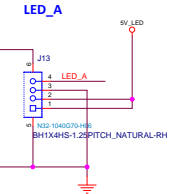
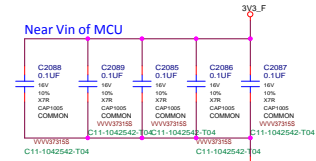
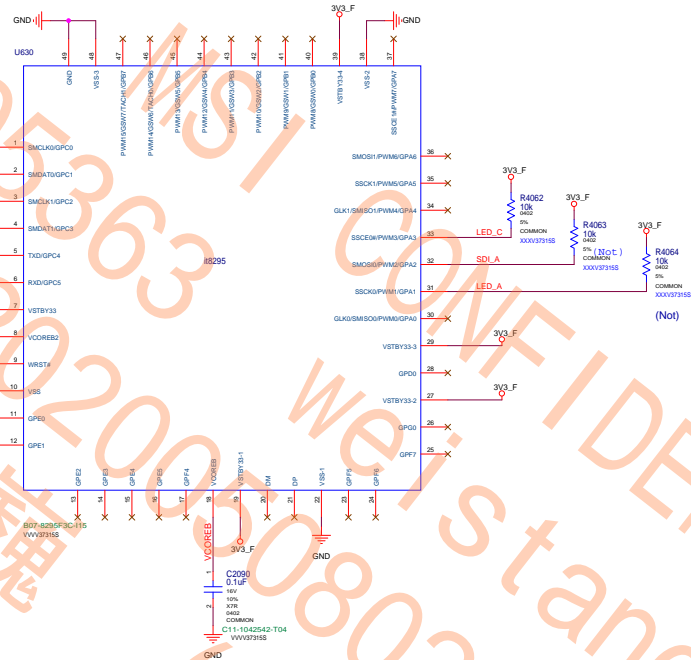
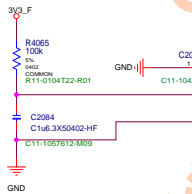
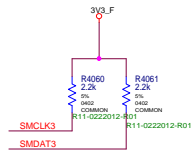
	MICRO-STAR INT'L CO.,LTD		
	MS-V373		
	Size	Document Description	Rev
	Custom	Page52LED & FAN HEADERS	2.1
Date: Saturday, June 15, 2019		Sheet	52 of 54

## Firmware Programming

## Debug



27.31,32,33,48  
27.31,32,33,48



## 5V\_LED

